PATENT APPLICATION

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Application No.: 09/486,556

Filed: February 29, 2000

Group Art Unit: 2841

Examiner: I. Patel

Docket No.: 105029

J. McCamish 10/3/02
Entered
J McMillan
11/1/02

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE THEREOF, CIRCUIT BOARD AND ELECTRONIC INSTRUMENT

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 1-29 without prejudice to or disclaimer of the subject matter contained therein.

Please add new claims 30-85 as follows:

--30. A method of manufacturing a semiconductor device, comprising:

mounting a semiconductor chip on a substrate, said semiconductor chip having electrodes, said substrate having an interconnect pattern formed thereof and a protective layer covering at least a part of said interconnect pattern, said semiconductor chip mounted on said substrate such that an edge of said semiconductor chip does not overlap with said protective layer;

electrically connecting said electrodes to said interconnect pattern; and

adhering said semiconductor chip to said substrate by an adhesive, said adhesive provided on said substrate from a region in which said semiconductor chip is mounted to said protective layer.--

--31. The method of manufacturing a semiconductor device as defined in claim 30, wherein said interconnect pattern and said electrodes are electrically connected by conductive particles dispersed in said adhesive.--

--32. The method of manufacturing a semiconductor device as defined in claim 30, wherein before adhering said semiconductor chip to said substrate, said adhesive is previously disposed on a surface of said semiconductor chip on which said electrodes are formed.--

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--33. The method of manufacturing a semiconductor device as defined in claim 30, wherein before adhering said semiconductor chip to said substrate, said adhesive is previously disposed on a surface of said substrate on which said interconnect pattern is formed.--

--34. The method of manufacturing a semiconductor device as defined in claim 30, wherein said adhesive is a thermosetting adhesive.--

--35. The method of manufacturing a semiconductor device as defined in claim 34, wherein said adhesive is spread out beyond said semiconductor chip and

wherein heat is applied between said semiconductor chip and said substrate to cure said adhesive between said semiconductor chip and said substrate;

said manufacturing method further comprising applying heat to a part of said adhesive not completely cured.--

--36. The method of manufacturing a semiconductor device as defined in claim 35, wherein said adhesive is heated by a heating apparatus.--

--37. The method of manufacturing a semiconductor device as defined in claim 36, wherein a nonadhesive layer having improved nonadhesive properties with respect to said adhesive is interposed between said heating apparatus and said adhesive, before heating said adhesive.--

--38. The method of manufacturing a semiconductor device as defined in claim 37, wherein said nonadhesive layer is provided on said heating apparatus.--

--39. The method of manufacturing a semiconductor device as defined in claim 37, wherein said nonadhesive layer is provided on said adhesive.--

--40. The method of manufacturing a semiconductor device as defined in claim 35, wherein said adhesive is heated by a non-contact method.--

--41. The method of manufacturing a semiconductor device as defined in claim 35, further comprising a reflow step of forming solder balls on said substrate to be connected to said interconnect pattern,

wherein said step of applying heat is carried out in said reflow step.--

--42. The method of manufacturing a semiconductor device as defined in claim 35, further comprising a reflow step of electrically connecting an electronic component other than said semiconductor chip to said interconnect pattern,

wherein said step of applying heat is carried out in said reflow step.--

--43. The method of manufacturing a semiconductor device as defined in claim 30, further comprising cutting said substrate together with said adhesive in a region not in contact with said semiconductor chip after adhering said semiconductor chip to said substrate.--

--44. The method of manufacturing a semiconductor device as defined in claim 43, wherein said substrate is cut in a region outside an edge of said interconnect pattern.--

--45. The method of manufacturing a semiconductor device as defined in claim 43, wherein a whole of said adhesive is cured before said substrate is cut together with said cured adhesive.--

--46. The method of manufacturing a semiconductor device as defined in claims 30, wherein said adhesive is caused to surround at least a part of a lateral surface of said semiconductor chip during adhering said semiconductor chip to said substrate.--

--47. The method of manufacturing a semiconductor device as defined in claim 46, wherein said adhesive is provided at a thickness greater than an interval between said semiconductor chip and said substrate, and is spread out beyond said semiconductor chip by applying pressure between said semiconductor chip and said substrate.--

--48. The method of manufacturing a semiconductor device as defined in claims 30, wherein said adhesive includes a shading material.--

Cont'd E1

--49. The method of manufacturing a semiconductor device as defined in claim 30, wherein said substrate is provided previously covered by said protective layer except said region in which said semiconductor chip is mounted and a periphery of said region.--

--50. A method of manufacturing a semiconductor chip, comprising:

providing an adhesive over a substrate which includes an interconnect pattern formed thereover and a protective layer covering said interconnect pattern, said substrate having a first region on which a semiconductor ship is mounted and a second region which surrounds said first region, said protective layer having and edge portion on said interconnect pattern in said second region, said edge portion, said first region and a part of said interconnect pattern below said edge portion covered with said adhesive; and

providing said semiconductor chip including electrodes onto said first region to electrically connect said electrodes to said interconnect pattern.--

--51. The method of manufacturing a semiconductor device as defined in claim 50, wherein said interconnect pattern and said electrodes are electrically connected by conductive particles dispersed in said adhesive.--

--52. The method of manufacturing a semiconductor device as defined in claim 50, wherein said adhesive is a thermosetting adhesive.--

--53. The method of manufacturing a semiconductor device as defined in claim 52, wherein said adhesive is spread out beyond said semiconductor chip, and wherein heat is applied between said semiconductor chip and said substrate to cure said adhesive between said semiconductor chip and said substrate;

said manufacturing method further comprising applying heat to a part of said adhesive not completely cured.--

--54. The method of manufacturing a semiconductor device as defined in claim 53, wherein said adhesive is heated by a heating apparatus.--

--55. The method of manufacturing a semiconductor device as defined in claim 54, wherein a nonadhesive layer having improved nonadhesive properties with respect to said adhesive is interposed between said heating apparatus and said adhesive, before heating said adhesive.--

--56. The method of manufacturing a semiconductor device as defined in claim 55, wherein said nonadhesive is provided on said heating apparatus.--

--57. The method of manufacturing a semiconductor device as defined in claim 55, wherein said nonadhesive layer is provided on said adhesive.--

--58. The method of manufacturing a semiconductor device as defined in claim 53, wherein said adhesive is heated by a non-contact method.--

--59. The method of manufacturing a semiconductor device as defined in claim 53, further comprising a reflow step of forming solder balls on said substrate to be connected to said interconnect pattern,

wherein said step of applying heat is carried out in a reflow step.--

--60. The method of manufacturing a semiconductor device as defined in claim 53, further comprising a reflow step of electrically connecting an electronic component other then said semiconductor chip to said interconnect pattern,

wherein said step of applying heat is carried out in said reflow step.--

--61. The method of manufacturing a semiconductor device as defined in claim 50, further comprising cutting said substrate together with said adhesive in a region not in contact with said semiconductor chip after adhering said semiconductor chip to said substrate.--

--62. The method of manufacturing a semiconductor device as defined in claim 61, wherein said substrate is cut in a region outside an edge of said interconnect pattern.--

--63. The method of manufacturing a semiconductor device as defined in claim 61, wherein a whole of said adhesive is cured before said substrate is cut together with said cured adhesive.--

--64. The method of manufacturing a semiconductor device as defined in claim 50, wherein said adhesive is caused to surround at least a part of a lateral surface of said semiconductor chip during adhering said semiconductor chip to said substrate.--

--65. The method of manufacturing a semiconductor device as defined in claim 64, wherein said adhesive is provided at a thickness greater than an interval between said semiconductor chip and said substrate, and is spread out beyond said semiconductor chip by applying pressure between said semiconductor chip and said substrate.--

--66. The method of manufacturing a semiconductor device as defined in claim 50, wherein said adhesive includes a shading material.--

--67. The method of manufacturing a semiconductor device as defined in claim 50, wherein said substrate is provided previously covered by said protective layer except said first region and a periphery of said first region.--

--68. A semiconductor device, comprising:

a substrate, said substrate having an interconnect pattern formed thereover, said substrate having a protective layer covering at least a part of said interconnect pattern;

a semiconductor chip, said semiconductor chip having electrodes, said electrodes electrically connected to said interconnect pattern, said semiconductor chip

mounted on said substrate such that an edge of said semiconductor chip does not overlap with said protective layer; and

an adhesive, said adhesive adhering said semiconductor chip to said substrate, said adhesive provided on said substrate from a region in which said semiconductor chip is mounted to said protective layer.--

--69. The semiconductor device as defined in claim 68, wherein conductive particles are dispersed in said adhesive to form an anisotropic conductive material.--

--70. The semiconductor device as defined in claim 69, wherein said anisotropic conductive material is provided to cover a whole of said interconnect pattern.--

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--71. The semiconductor device as defined in claim 68, wherein said adhesive covers at least a part of a lateral surface of said semiconductor chip.--

--72. The semiconductor device as defined in claim 68, wherein said adhesive includes a shading material.--

--73. The semiconductor device as defined in claim 68, wherein said protective layer is provided to cover said substrate except said region in which said semiconductor chip is mounted and a periphery of said region.--

--74. A semiconductor device, comprising:

a substrate including an interconnect pattern formed thereover and a protective layer covering said interconnect pattern, said substrate having a first region on which a semiconductor chip is mounted and a second region which surrounds said first region, said protective layer having an edge portion in said second region;

said semiconductor chip including electrodes electrically connected to said interconnect pattern; and

an adhesive between said substrate and said semiconductor chip, the adhesive covering said edge portion, said first region and a part of said interconnect pattern below said edge portion.--

--75. The semiconductor device as defined in claim 74, wherein conductive particles are dispersed in said adhesive to form an anisotropic conductive material.--

--76. The semiconductor device as defined in claim 75, wherein said anisotropic conductive material is provided to cover a whole of said interconnect pattern.--

--77. The semiconductor device as defined in claim 74, wherein said adhesive covers at least a part of a lateral surface of said semiconductor chip.--

Cont'd

--78. The semiconductor device as defined in claim 74, wherein said adhesive includes a shading material.--

--79. The semiconductor device as defined in claim 74, wherein said protective layer is provided to cover said substrate except said first region and a periphery of said first region.--

--80. A semiconductor device manufactured by the method as defined in claim 30.--

--81. A semiconductor device manufactured by the method as defined in claim 50.--

--82. A circuit board on which is mounted the semiconductor device as defined in claim 68.--

--83. A circuit board on which is mounted the semiconductor device as defined in claim 74.--

--84. An electronic instrument having the semiconductor device as defined in claim 68.--

--85. An electronic instrument having the semiconductor device as defined in claim 74.--

REMARKS

Claims 30-85 are pending. By this Amendment, claims 1-29 are cancelled without prejudice or disclaimer, and new claims 30-85 are added. No new matter is introduced. Applicant respectfully requests prompt examination and allowance of pending claims in due course.

Respectfully submitted,

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JAO:PT/sld

Attachment:
Amendment Transmittal

Date: June 6, 2002

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